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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,837	10/30/2003	Li-Chyn Wang	MSCP0016USA	2836

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,837	WANG, LI-CHYN	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is responsive to the communication filed on 3/30/06.

2. Claims 1-5, 7-9 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Response to Arguments

4. Applicant's arguments with respect to claim 1-5, 7-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki U.S. Patent 5,995,454 in view of Tran et al. U.S. Patent 5,224,010.

9. As per claim 1, Yamaki discloses a method for enabling a computer to self-start comprising:

selecting a predetermined time for self-start when the computer is on [col. 4 lines 19-28];

adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 4 lines 36-47; col. 5 lines 35-37; col. 6 lines 51-59];

powering the computer off [col. 5 lines 33-34]; and

providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 4 lines 47-52];

sending a power on signal to the power supply via the power supply connector on the motherboard [col. 4 lines 48-52];

and starting the computer [col. 7 lines 14-21].

However, Yamaki does not explicitly teach the powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer.

Tran et al. teach another method related to the field of data processing systems, and is more particularly directed to power supply supervisor circuit in the data processing systems. Specifically, Tran et al. teaches

powering of the voltages of pins of the power supply connector to appropriate levels [col. 10 lines 18-44];

checking if the voltage in the pins of the power supply connector are stable [col. 10 line 45-67];

sending a power good signal from the power supply to a processor of the computer [col. 10 line 65 to col. 11 line 3]; and

stating the computer upon receiving the power good signal [col. 11 lines 3-6; col. 6 lines 27-37].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the detecting of the power good signal from the power supply before power on the computer of Tran et al. in order to reduce loss of data or other functional system errors caused by unstable or varying power supply voltages [col. 1 lines 15-19].

10. Claims 2-3, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki as applied to claim 1 above, and further in view of Lin et al. US 20030095044.

11. As per claim 2, Yamaki teaches the enabling the power supply controller (PSC) wherein the PSC chipset is able to respond to a matching signal send from the RTC/NVRAM chip when the computer is off [col. 4 lines 47-52]. However, Yamaki does not teach enabling the system control interrupt bit in a Southbridge chip set of the computer.

Lin et al. teach another method that enabling the computer to turned on via a wireless remote controller. Specifically, Lin et al. teach enabling the System Control Interrupt (SCI) bit

in a Southbridge chip set of the computer; wherein the Southbridge chipset is able to respond to a matching signal sent from a wireless remote controller when the computer is off [paragraph 0026 and 0027].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the Southbridge of Lin et al. since the Southbridge chipset is well know the art of computer architect.

12. As per claim 3, Yamaki teaches the BIOS is employed to execute various processes including the system power-on process and power off process [col. 4 lines 53-55]. Therefore, it is obvious to one of ordinary skill in the art that BIOS is also employ to enable the SCI bit in the Southbridge.

13. As per claim 5, Yamaki teaches activating the PSC in the computer to send a power on signal in response to a match between the clock value of the RTC/NVRAM chip and the alarm setting stored in the memory of the RTC/NVRAM chip [fig. 1]; and

Lin et al. teach activating the SCI pin of a Southbridge chipset in the computer to send a power on signal in response to a access signal. Therefore, it is obvious to one of ordinary skill in the art to combine the teachings of Yamaki and Lin et al. to obtain the invention as specified in claim 5.

14. Claims 1, 4, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomiyasu in view of Tran et al.

15. As per claim 1, Tomiyasu discloses a method for enabling a computer to self-start comprising:

selecting a predetermined time for self-start when the computer is on [fig. 9; col. 6 lines 42-48];

adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 6 lines 49-53];

powering the computer off [inherent]; and

providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 7 lines 3-20];

sending a power on signal to the power supply via a power supply connector on a motherboard of the computer; and

starting the computer.

However, Tomiyasu does not explicitly teach

powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer; and

stating the computer upon receiving the power good signal.

Tran et al. teach another method related to the field of data processing systems, and is more particularly directed to power supply supervisor circuit in the data processing systems. Specifically, Tran et al. teaches

powering of the voltages of pins of the power supply connector to appropriate levels [col. 10 lines 18-44];

checking if the voltage in the pins of the power supply connector are stable [col. 10 line 45-67];

sending a power good signal from the power supply to a processor of the computer [col. 10 line 65 to col. 11 line 3]; and

stating the computer upon receiving the power good signal [col. 11 lines 3-6; col. 6 lines 27-37].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the detecting of the power good signal from the power supply before power on the computer of Tran et al. in order to reduce loss of data or other functional system errors caused by unstable or varying power supply voltages [col. 1 lines 15-19].

16. As per claim 4, Tomiyasu discloses sending a matching signal from the RTC/NVRAM chip by changing the value of the 11^{th} byte in the memory of the RTC/NVRAM chip [col. 5 lines 46-57 – see fig. 6 for byte position].

17. As per claim 7, Tomiyasu discloses using an application of an operating system in the computer to select the predetermined time [fig. 9].

18. As per claim 8, Tomiyasu discloses the operating system employs a driver to relay the selected predetermined time to the BIOS [inherent - col. 6 lines 49-53; col. 3 lines 47-49].

19. As per claim 9, Tomiyasu discloses the adjusting of the alarm setting further comprises:

employing the BIOS to adjust the alarm setting in the memory of the RTC/NVRAM chip [col. 6 lines 49-53; col. 3 lines 47-49].

20. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki U.S. Patent 5,995,454 in view of Stapleton et al. U.S. patent 6,574,577.

21. As per claim 1, Yamaki discloses a method for enabling a computer to self-start comprising:

selecting a predetermined time for self-start when the computer is on [col. 4 lines 19-28];

adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 4 lines 36-47; col. 5 lines 35-37; col. 6 lines 51-59];

powering the computer off [col. 5 lines 33-34]; and

providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 4 lines 47-52];

sending a power on signal to the power supply via the power supply connector on the motherboard [col. 4 lines 48-52];

and starting the computer [col. 7 lines 14-21].

However, Yamaki does not explicitly teach the powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer.

Stapleton et al. teach another method relates to a circuit to indicate the status of a supply voltage. Specifically, Stapleton et al. teaches

powering of the voltages of pins of the power supply connector to appropriate levels [col. 2 lines 51-59];

checking if the voltage in the pins of the power supply connector are stable [col. 2 lines 27-37];

sending a power good signal from the power supply to a processor of the computer [col. 2 lines 38-50]; and

stating the computer upon receiving the power good signal [inherent].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the detecting of the power good signal from the power supply before power on the computer of Stapleton et al. in order to reduce loss of data or other functional system errors caused by unstable or varying power supply voltages during start-up [col. 1 lines 15-19].

22. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaki U.S. Patent 5,995,454 in view of Mar et al. U.S. Patent 6,792,553.

23. As per claim 1, Yamaki discloses a method for enabling a computer to self-start comprising:

selecting a predetermined time for self-start when the computer is on [col. 4 lines 19-28];

adjusting an alarm setting stored in a memory of an RTC/NVRAM chip according to the predetermined time [col. 4 lines 36-47; col. 5 lines 35-37; col. 6 lines 51-59];

powering the computer off [col. 5 lines 33-34]; and

providing electrical power with a power supply if a clock value of the RTC/NVRAM chip matches the alarm setting [col. 4 lines 47-52];

sending a power on signal to the power supply via the power supply connector on the motherboard [col. 4 lines 48-52];

and starting the computer [col. 7 lines 14-21].

However, Yamaki does not explicitly teach the powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer.

Mar et al. teach another method relates to sequentially power on the processors of the computer system. Specifically Mar et al. teach

powering of the voltages of pins of the power supply connector to appropriate levels;

checking if the voltage in the pins of the power supply connector are stable;

sending a power good signal from the power supply to a processor of the computer; and

stating the computer upon receiving the power good signal [abstract].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Yamaki with the detecting of the power good signal from the power supply before power on the computer of Mar et al. in order to reduce loss of data or other functional system errors caused by unstable or varying power supply voltages during start-up [col. 1 lines 15-19].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran